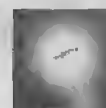


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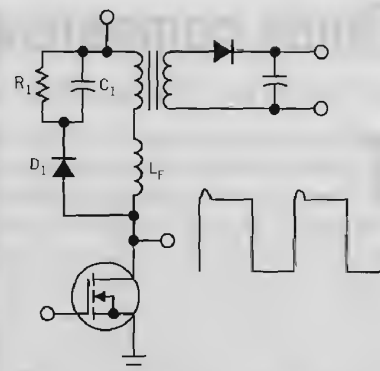
## Slow diodes or handy timing devices?

Louis Vleminckx, Belgacom, Evere, Belgium

**M**OST DESIGNERS consider slowness in diodes to be an imperfection or a limitation. Why not take a more positive view of the situation? After all, a zener or an avalanche diode is no more than a diode with a limited breakdown voltage, and you can view a varactor as a diode with a large and nonlinear parasitic capacitance. Similarly, could you view the slowness of a diode as a property or even a feature? For example, consider a PIN diode. Few people are aware that the key

property of a PIN diode is indeed its slowness; without it, it would generate large amounts of distortion and require a larger control current to function properly. You can put this ability of slow diodes to store large amounts of electrical charge to good use in a variety of other circuits. **Figure 1** shows how to generate dead time using such diodes. A PWM sandcastle (stepped) waveform feeds a half-bridge. When the control signal reverses its polarity, a negative bias appears immediately on  $Q_1$ , but  $D_2$  cannot instantly cease conducting and short-circuits the base drive to  $Q_2$  during all of its reverse recovery time. The advantage of generating a dead time in this way lies in the fact that you need include only a small safety margin: The phenomena governing the recovery time of a diode are similar to those resulting in storage times in power devices. In particular, they both display a strong positive-temperature coefficient, for which this scheme compensates. The ability to operate at duty cycles close to 100% allows a better usage of the power components, translating into savings and higher performance: A universal-input supply, for instance, can operate at lower supply voltages.

**Figure 2** shows another example. This standard clamping circuit protects the switching transistor of a flyback converter against the voltage spike generated by the imperfect coupling between the primary and the secondary windings of the transformer. In an equivalent schematic, this scenario translates into a leakage inductance,  $L_F$ , in series with the primary winding. The circuit works in the following way: Each time the transistor turns off, the current in the leakage inductance continues to flow, but  $D_1$  intercepts it and "redirects" it to  $C_1$ .  $C_1$  has a large enough capacitance that cycle-to-cycle variations do not influence it. The average voltage on  $C_1$  results from a balance between the charging input from the leakage inductance and the current that bleeds from  $R_1$ . Usually,  $D_1$  is a fast diode, but, if you substitute it with a slow one, interesting things happen: Instead of switching off when the voltage on  $C_1$  reaches its peak,  $D_1$  continues to conduct, thus transferring back charge and ener-



**Figure 2** In this circuit, a slow diode protects the switching transistor from destructive voltage transients.

gy from  $C_1$  to the transformer and ultimately to the load. The overall efficiency is therefore better, and  $R_1$  can have higher resistance and can be smaller. Added to the lower cost of a standard diode versus a fast one, the method provides non-negligible benefits.

It is preferable to select a diode with a recovery time as long as possible. Popular types, such as the 1N400X series, have recovery times of approximately 2.5  $\mu\text{sec}$ , but some models reach more than 5  $\mu\text{sec}$ . Ideally,  $C_1$  and  $L_F$  should resonate at a period equal to twice the diode's recovery

**Figure 1**

You can use slow diodes to generate dead time in a half-bridge configuration.

property of a PIN diode is indeed its slowness; without it, it would generate large amounts of distortion and require a larger control current to function properly. You can put this ability of slow diodes to store large amounts of electrical charge to good use in a variety of other circuits. **Figure 1** shows how to generate dead time using such diodes. A PWM sandcastle (stepped) waveform feeds a half-bridge.

In a classical implementation, you must insert dead time in the control circuitry to avoid the simultaneous conduction of the two transistors when the duty cycle approaches 100%. This dead time is a standard feature of PWM-control ICs. If you use slow diodes for  $D_1$  and  $D_2$ , you need no dead time. If, for example,  $Q_1$  receives a positive base, or gate, drive and is therefore conducting,  $D_2$  becomes forward-bi-

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time. When the component values are nearly optimum,  $R_1$  can have a large value, its only role being to provide a "seed" current to prime the circuit. You pay a small penalty for these advantages: The peak clamping voltage increases by several volts, because you must add the posi-

itive cycle of the resonance to the average clamping voltage and because slow diodes often exhibit a slightly poorer forward-recovery characteristic than do their fast counterparts. This characteristic results in a step of several volts at the beginning of the conduction.

Normally, these small snags should pose no problem; you can substitute the new components in a design without any other change. The circuits in **figures 1** and **2** are only two examples, but you can apply the same useful principles to a variety of other circuits. □

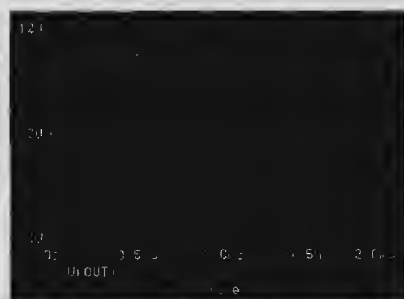
## Diode compensates distortion in amplifier stage

S Chekcheyev, Pridnestrovye State University, Moldova

**T**HE VOLTAGE AMPLIFIER in **Figure 1** exhibits smaller nonlinear distortion than does the conventional amplifier in **Figure 2**. Diode  $D_1$  compensates for the distortion inherent in the npn transistor. The voltage gain of a common-emitter amplifier depends on the transconductance of the transistor. The transconductance of the bipolar transistor is as follows:

$$S = \frac{eI}{k(273 + T^{\circ}\text{C})} = nI,$$

where  $e$  is the charge of an electron,  $k$  is Boltzmann's constant (approximately  $1.38 \times 10^{-23} \text{ J/K}$ ),  $T^{\circ}\text{C}$  is temperature in degrees Celsius,  $I$  is the emitter current, and  $n = e/[k(273 + T^{\circ}\text{C})]$ . So, the transconductance is proportional to the emit-



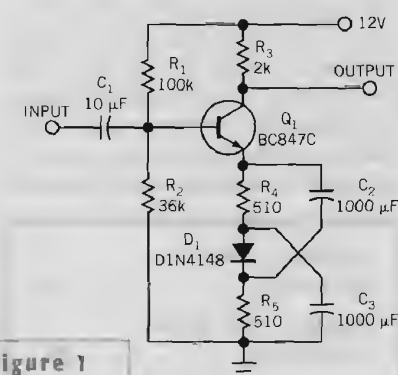
**Figure 3** Nonlinearity of the transconductance of  $Q_1$  results in this distorted waveform.



**Figure 4** The diode in the circuit of **Figure 1** produces varying, beneficial, negative feedback.

ter half-cycle (**Figure 3**).

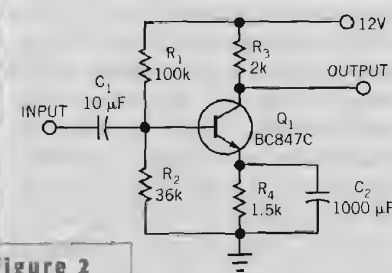
The dynamic resistance of diode  $D_1$  in **Figure 1** is inversely proportional to the instantaneous current. That dynamic resistance forms part of the negative-feedback circuit of the amplifier. The average current of diode  $D_1$  is equal to the average emitter current of transistor  $Q_1$ . However, the instantaneous current of  $D_1$  becomes smaller, and the instantaneous dynamic resistance of  $D_1$  becomes larger when the instantaneous emitter current of  $Q_1$  becomes larger, and vice versa. Therefore, the negative feedback becomes stronger during the negative half-cycle of the output signal. As a result, the output signal of the amplifier be-



**Figure 1**

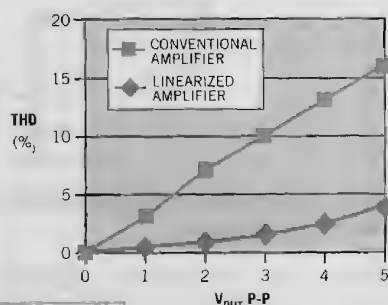
The addition of a simple diode in the emitter circuit yields the symmetric waveform of **Figure 4**.

ter current. Consequently, the instantaneous voltage-gain coefficient of the conventional common-emitter amplifier is proportional to the instantaneous emitter current. As a result, the negative half-cycle of the output signal gets more amplification than does the posi-



**Figure 2**

This amplifier circuit produces the distorted waveform of **Figure 3**.



**Figure 5** The linearized amplifier produces less than one-third the harmonic distortion of the conventional amplifier.

comes more symmetric (**Figure 4**). The circuits in **figures 1** and **2** have the same average collector current and the same load resistance. **Figures 3** and **4** show the results of their PSpice simulation. The amplitude of the output signal is 5V p-p in both cases with a 1-kHz sinusoidal signal applied to the input. You can see that the linearized amplifier yields a more symmetrical output signal. **Figure 5** gives the quantitative results of the simulations. The improvement in harmonic distortion accrues because of the suppression of the even harmonics in the output of the linearized amplifier. □